

U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	SN DK.A06US5	09/759,119
	Applicant(s)	Conf. No.
(Form PTO-1449)	Harari et al.	1201
	Filing Date	Group
	January 11, 2001	2827

## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
TN	1	4,090,258	5/16/78	Cricchi			
TN	2	4,149,270	4/10/79	Cricchi et al.			
TN	3	4,181,980	1/1/80	McCoy			
TN	4	4,253,059	2/24/81	Bell et al.			
TN	5	4,272,830	6/9/81	Moench			
TN	6	4,279,024	7/14/81	Schenk			
TN	7	4,393,475	9/1/81	Stark			
TN	8	4,393,475	7/12/83	Kitagawa et al.			
TN	9	4,415,992	11/15/83	Adlhoch			
TN	10	4,460,982	7/17/84	Gee et al.			
TN	11	4,475,194	10/2/84	La Valee et al.			
TN	12	4,495,602	1/22/85	Sheppard			

## Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
TN	13	GB2061651	1981	United Kingdom				
TN	14	GB2029145	1980	United Kingdom				
TN	15	JP6225769	1988	Japan			X	
TN	16	JP5931158	1984	Japan				X
TN	17	DE363782	1987	Germany			Abstract	

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TN	18	Bleiker et al., "A Four State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, Vol. Sc-22. No. 3, June 1987, pp.460-463.
TN	19	Torelli et al., "An Improved Method for Programming A Word Erasable EEPROM", Alta Frequenza, Vol. 52, Nov.- Dec. 1983, No. 6, pp. 487-494.
TN	20	Stark, "Two Bits Per Cell ROM", Digest of Papers Spring COMCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.

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TN	21	4,586,163	4/29/86	Koike			
TN	22	4,612,629	9/16/86	Harari			
TN	23	4,677,590	6/30/87	Arakawa			
TN	24	4,718,041	1/5/88	Baglee et al.			
TN	25	4,733,394	3/22/88	Giebel			
TN	26	4,752,929	6/21/88	Kantz			
TN	27	4,779,272	10/18/88	Kohda et al.			
TN	28	4,799,195	1/17/89	Iwahashi et al.			
TN	29	4,807,188	2/21/89	Casagrande			
TN	30	4,890,231	2/28/89	Shannon et al.			
TN	31	4,811,294	3/7/89	Kobayashi et al.			

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		Document	Date	Country	Class	Subclass	Yes	No
TN	32	DE3831538	1989	Germany			Abstract	
TN	33	JP62-188100	1987	Japan			X	
TN	34	JP0123878	1989	Japan				
TN	35	JP0146949	1989	Japan				

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TN	36	Furuyama et al., "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1-4.4.4.
TN	37	Krick, "Three-State MNOS FET Memory Array", IBM Technical Disclosure Bulletin, Vol. 18, No. 12, May 1976, pp. 4192-4193.
TN	38	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin, Vol. 24, No. 7A, Dec. 1981, pp. 3311-3314, 4193.

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TN	39	4,870,618	9/26/89	Iwashita			
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TN	41	4,956,816	7/24/90	Atsumi et al.			
TN	42	4,980,861	12/25/90	Herd et al.			
TN	43	4,999,813	3/12/91	Ohtsuka et al.			
TN	44	5,003,510	3/26/91	Kamisaki			
TN	45	5,053,990	10/1/91	Kriefels et al.			
TN	46	5,095,344	3/10/92	Harari			
TN	47	5,136,021	11/10/92	Mehrota et al.			
TN	48	5,297,148	3/22/94	Harari et al.			
TN	49	5,357,462	10/18/94	Tanaka et al.			

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TN	50	Horiguchi et al. "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVEL/CELL storage", IEEE Journal of Solid-State Circuits, Vol. 23, Feb.1998, No.1, pp. 27-33.
TN	51	Masuoka et al. "A 256-KBIT Falsh EEPROM Using Triple-Polysilicon Technology", IEEE Journal of Solid-State Circuits, Vol. SC-22, No.4, pp.548-552, New York, USA, August 1987.
TN	52	Berenga et al. "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78", February 17, 1978, pp.196-197.
TN	53	Kynett et al. "An In-System Reprogrammable 32K X 8 CMOS Flash Memory", IEEE Journal of Solid-State-Circuits, Vol. 23, No.5, Log Number 8822443, October 1988, pp. 1157-1163.
TN	54	Klingman, "Microprocessor Systems Design", Prentice-Hall, Inc. pp.30-31, 1977.
TN	55	SGS-ATES "Excerpts From a 1983 Data Book", SGS-Ates Group, 45 pp., Nov. 1983.
TN	56	Torelli et al., "Non-Volatile Station Memory and Remote-Control Receiver and Memory Display Driver", IEEE Transactions on Consumer Electronics, Vol. CE-29, No.3, pp.103-13, August 1983.
TN	57	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver in a Single Chip", IEEE Digest of Technical Papers, CAT. No.: 83CH1872-1, 2 pp., June 8, 1983

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TN	59	5,602,987	2/11/97	Harari et al.			
TN	60	4,959,812	9/25/90	Momodomi et al.			
TN	61	4,939,690	7/3/90	Momodomi et al.			
TN	62	4,996,669	2/26/91	Endoh et al.			
TN	63	5,163,021	1992	Mehrotra et al.			
TN	64	5,172,338	1992	Mehrotra et al (Reexamination)			
TN	65	5,657,270	1997	Ohuchi et al.			
TN	66	5,793,696	8/11/98	Tanaka et al.			
TN	67	5,831,903	11/03/98	Ohuchi et al.			

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TN	68	Caironi et al., "A TV Frequency Synthesis System With a Single Chip Microprocessor Interface Including Non-Volatile Memory", IEEE Transactions on Consumer Electronics", Vol. CE-28, No.3, pp.363-71, August 1982.
TN	69	Torelli, "An LSI Technology Fully Compatible EAROM Cell", Component Elettronico SpA, No. 6, Vol. LI, 7 pp. 1982.
TN	70	Torelli et al., PLL2K-PLL Frequency Synthesizer for 30 Programs", SGS-ATES, Technical Note #152, pp.1-16, 1982.
TN	71	Torelli et al. "Single Chip, 16 Station TV Digital Tuning System", SGS Technical Note #170, pp.1-19, 1984.
TN	72	Scrocchi et al. "EPM32-Electronic Program Memory System for TV (32 stations)" SGS-ATES, Technical Note#153, pp. 1-19, 1982.
TN	73	SGS-ATES. "PLL TV Microcomputer interface", SGA-ATES, MOS Integrated Circuits/M206, 15 pp. June 1982.

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## U.S. Published Patent Application Documents

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## Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No

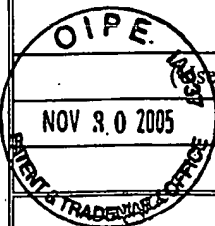
## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

TN	Office Action for Application No. 09/606,911 mailed November 9, 2005, 15 pages.

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TN	5,034,922	7/23/91	Burgess			

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## Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

TN	Office Action for Application No. 09/635,597 mailed August 22, 2005, 12 pages.

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